IN-SITU LINER FORMATION DURING REACTIVE ION ETCH

FIELD OF THE INVENTION

The invention relates generally to semiconductor integrated circuit manufacturing and, more particularly, to in-situ liner formation during reactive ion etching ("RIE").

BACKGROUND OF THE INVENTION

As wafer fabrication design rules reduce to 0.15 μm linewidths and below, the increased packing density of devices on a chip permits more electrical signal speed from device to device. This density leads to improved chip performance. However, this improved chip performance is only possible if the interconnect system between the devices is optimized. Narrower linewidths lead to increased line resistance. Tightly spaced conductor lines with a dielectric material between them act as capacitors, leading to a degradation in performance from an increased resistance ("R") and capacitance ("C"). If either or both of these parameters are reduced, then the signal delay reduces, leading to increased chip performance. One method for reducing interconnect resistance is to increase the conductor cross section. However, this contradicts the goal of increased packing density since wider conductors will require more space. Additionally, smaller integrated circuit ("IC") feature sizes are not achievable with larger linewidths. This has lead the semiconductor industry to search for alternative materials and processes.

Conventionally, aluminum ("Al") has been used by the semiconductor industry as an interconnect material. Recently, copper ("Cu") has been introduced as an interconnect material. The use of copper metallization provides improved performance and reliability

over aluminum. Copper can lower the interconnect resistance, lowering R and the overall signal delay. Additionally, copper enables the creation of smaller linewidths with the ability to carry the same amount of current as large linewidths, permitting a tighter packing density on each metal level The optimum improvement to RC signal delay is gained when R is reduced and C is lowered by using a low-*k* dielectric, along with thinner barrier metals.

However, semiconductor processing with copper metallurgy can be complicated, for a number of reasons. One, copper diffuses quickly into oxides and silicon. Therefore, copper must be isolated from the surrounding inter-level dielectric ("ILD"). If the copper reaches the silicon substrate, it will significantly degrade device performance. Additionally, copper cannot be easily patterned using regular plasma etching techniques. Copper dry etching does not produce a necessary volatile by-product during the chemical reaction as required for economical dry etching. Furthermore, copper oxidizes quickly in air at low temperatures (i.e., $< 200^{\circ}$ C) and does not form a protective layer to stop further oxidation. Therefore, to form copper interconnect wiring, damascene processing has been introduced. Damascene processing eliminates the need to etch copper because a dielectric etch is used to define the critical line width and spacing, rather than the metal etch used with aluminum.

In a damascene process, both the vias and lines for each metal layer are created by etching holes and trenches in the ILD, depositing copper in the etched features and using CMP to remove excess copper. Damascene processing may include trench-first, via-first, and self-aligned etching. FIGURE 1 illustrates a known example of a damascene

process. In step **105**, an ILD oxide (e.g., a low-*k* material) is deposited on a wafer using, for example, plasma-enhanced chemical vapor deposition ("PECVD"). Next, in step **110**, one or more dielectric capping/hardmask layers are deposited on the ILD. In step **115**, a metal hardmask is deposited next. Feature (e.g., line or via) lithography is performed in step **120**, resulting in the structure of FIGURE 2. In step **125**, the feature is etched into the metal hardmask deposited in step **115** and, possibly, into one of the dielectric hardmask layers deposited in step **110**, resulting in the structure of FIGUREs 3 (with photoresist) and 4 (photoresist removed). In step **135**, the ILD is etched by RIE.

During the RIE step **135**, the sputter rate associated with the metal hardmask is finite but non-zero. In a dielectric etch chamber, sputter products from the metal hardmask can be expected to be involatile and will therefore stick to most surfaces. So, when the metal hardmask is exposed to the plasma during the RIE process, some redeposition of sputtered metallic products from the metal hardmask can be expected to occur inside the partially etched feature.

After RIE, in step **140**, a diffusion layer of barrier metal (e.g., tantalum and tantalum nitride) is deposited on the bottom and sidewalls of the trenches and vias. If the aforementioned sputtering and redeposition of the metal hardmask occurs during RIE, then it is typically necessary to remove the redeposition products from the etched feature (e.g., from the sidewalls and/or bottom of a trench) before the barrier deposition **140**. A copper seed layer is deposited onto the barrier metal in step **145**. Copper is then used to fill both the vias and trenches in step **150**. Finally, in step **155**, excess copper is removed

through surface planarization, such as CMP. The resulting surface is a planar structure with copper inlays forming the circuitry in the dielectric.

Because copper has high diffusity in silicon and silicon dioxide, which can destroy device performance, the aforementioned layer of barrier metal can be critical for copper metallurgy. Copper typically requires complete encapsulation by a thin-film barrier layer that functions as an adhesion promoter and as an effective diffusion barrier. For copper interconnect metallurgy, tantalum ("Ta"), tantalum nitride ("TaN"), and tantalum silicon nitride ("TaSiN") have been implemented as barrier metals. Heretofore, barrier metals have been deposited in a separate chamber as a separate processing step (Step **140**, FIGURE 1) after RIE (Step **135**, FIGURE 1). This subjects the low-*k* dielectric to an air break exposure, which can result in damage due to moisture uptake.

It is therefore desirable to provide a solution that reduces the possibility of damage to low-*k* dielectrics caused by exposure to air during damascene processing. Exemplary embodiments of the present invention exploit metal hardmask sputtering redeposition that occurs during RIE, thereby to produce the desired barrier layer during RIE while also avoiding air break exposure of the low-*k* dielectric.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and further advantages of the invention may be better understood by referring to the following description in conjunction with the accompanying drawings in which corresponding numerals in the different figures refer to the corresponding parts, in which:

FIGURE 1 illustrates a known damascene process;

FIGUREs 2-4 physically illustrate selected operations of FIGURE 1;

FIGURE 5 illustrates exemplary embodiments of a damascene process in accordance with the present invention; and

FIGUREs 6-8 physically illustrate an example of the RIE operation of FIGURE 5.

DETAILED DESCRIPTION

The present invention can reduce the possibility of damage to the low-*k* dielectrics caused by exposure to air during processing, such as (single or dual) damascene processing. Exemplary embodiments of the present invention can provide this by incorporating the deposition of a barrier layer into an RIE step. As used hereinbelow, the term metal liner or metallic liner refers to a liner that contains, but need not consist exclusively of, metal.

Exemplary embodiments of the present invention modify RIE parameters to form a metallic liner (or barrier layer) during the RIE step of damascene processing (i.e., in-situ) rather than applying the metallic liner as a separate processing step. FIGURE 5 illustrates exemplary embodiments of a damascene process in accordance with the present invention. FIGURE 5 shows that step **135** of FIGURE 1 can be replaced by step **335**, which includes RIE with in-situ barrier metal liner formation. Therefore, step **140** of FIGURE 1 is not needed, so operations can proceed directly from **335** in FIGURE 5 to **145** in FIGURE 1.

As mentioned above, during conventional RIE at **135** in FIGURE 1, although the selectivity to the metal hardmask is typically high, there is some erosion of the metal hardmask (e.g., by physical sputtering). The products that are formed as a result of the hardmask erosion are most likely non-volatile and will redeposit on any surface. Examples of such surfaces include the etch front and the sidewalls inside the damascene feature. Therefore, while the features are being etched, metallic products can be deposited onto the aforementioned surfaces. Conventional processing attempts to

minimize formation of these products because they may lead, for example, to micromasking, sidewall sloping, etch stop and polymerization of the surface. However, according to exemplary embodiments of the invention, by specific selection of the metal hardmask and the RIE discharge parameters (based on the RIE reactor and choice of feedgases), it is possible to produce, within the dielectric etch chamber, a desired RIE profile, while also using the metallic redeposition to produce a conformal metallic liner on both the sidewalls and the bottom of the etched feature. In other words, a metallic liner can be formed during RIE, in the RIE chamber. The metal hardmask is thus used as a sputter target for the liner deposition (which takes place in-situ during RIE).

An exemplary in-situ liner process in accordance with exemplary embodiments of the present invention can include a metal hardmask, for example TaN, as the liner target. In some exemplary embodiments, the addition of a fluorocarbon gas, such as CF_4, in the RIE process can trigger changes to the liner. The pairing of TaN and CF_4 can result in the deposition of a Ta-containing liner along feature sidewalls. By controlling discharge parameters, it is possible to control the sidewall angle of the RIE profile and, thus, the liner angle.

FIGUREs 6-8 physically illustrate an example of the RIE operation **335** of FIGURE 5. The physical changes illustrated in FIGUREs 6-8 begin with the metal hardmask exposed as illustrated in FIGURE 4. The beginning of the RIE process is shown in FIGURE 6, wherein the process of etching the trench into the dielectric begins. FIGURE 7 illustrates the detail portion **61** of FIGURE 6, that is, the redeposition of sputtered metallic products from the metal hardmask. FIGURE 8 illustrates the

completed feature, in this example a trench, with the metal liner produced by the sputtering redeposition of metallic particles from the metal hardmask. As mentioned above, according to exemplary embodiments of the invention, the redeposition is controlled to avoid negative effects such as micromasking and excessive sidewall sloping.

In some exemplary embodiments, the etch process illustrated in FIGUREs 5-8 is a two-step etch using a conventionally available etch tool (parallel plate, medium density plasma). The first step is to transfer the pattern of the metal hardmask into the dielectric hardmask underneath (see also FIGUREs 1-4). The second step is to etch the pattern into the dielectric. For the first step, the following exemplary parameters can be used with a TEL SCCM etch tool: low pressure in the range of 30 mT-100mT; total RF power (with some bias power in some embodiments) above approximately 800 watts; mid to high Ar flow rate 350-700 sccm; and aggressive chemistry with CF_4 (e.g., 10-45 sccm) and/or CHF_3 (e.g., 10-45 sccm), and O_2 (e.g., 10-30 sccm). In one example of the second step, again with a TEL SCCM tool, and assuming for this example an organic dielectric (either dense or porous), an etch gas mixture of N_2 (e.g., approximately 300 sccm) and H_2 (e.g., approximately 300 sccm) is used, the 30 mT-100mT pressure range is used, and the total RF power is maintained at a predetermined level (for example, in a TEL SCCM etch chamber, approximately 2000 watts at 60 MHz and approximately 1000 watts at 2 MHz) in order to have enough energy to sputter some of the metal hardmask to provide the in-situ formation of the metal liner during the RIE process. With the exception of the RIE

parameters specified above, the RIE process according to the invention can utilize conventionally known RIE techniques.

In addition to the exemplary advantages described above, by eliminating the need for a separate liner deposition step after etching, in-situ liner deposition reduces turn around time, cost, and other related factors in semiconductor integrated circuit manufacturing.

Although exemplary embodiments of the invention are described above in detail, this does not limit the scope of the invention, which can be practiced in a variety of embodiments. For example, although specific examples of etching an organic dielectric are described above, workers in the art will recognize that the invention is applicable to either organic or inorganic dielectrics, whether dense or porous. Also, although a TEL SCCM etch tool is specified in some examples above, workers in the art will recognize that other etch tools, for example a LAM HPT etch tool, can be used to practice the invention.